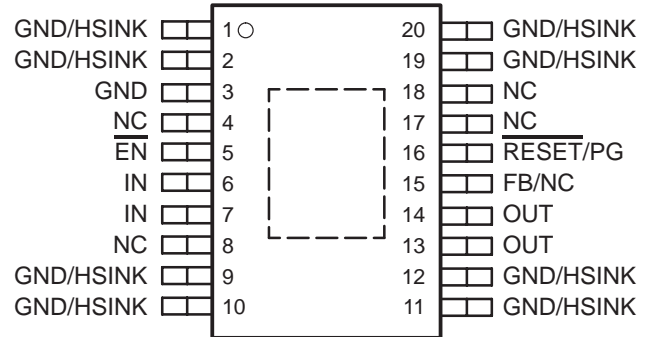


- Open Drain Power-On Reset With 200 ms Delay (TPS777xx)
- Open Drain Power Good (TPS778xx)
- 750-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V Fixed Output and Adjustable Versions
- Dropout Voltage to 260 mV (Typ) at 750 mA (TPS77x33)
- Ultralow 85 μA Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

description

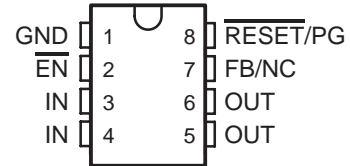
TPS777xx and TPS778xx are designed to have a fast transient response and be stable with a 10 μF low ESR capacitor. This combination provides high performance at a reasonable cost.

PWP PACKAGE
(TOP VIEW)

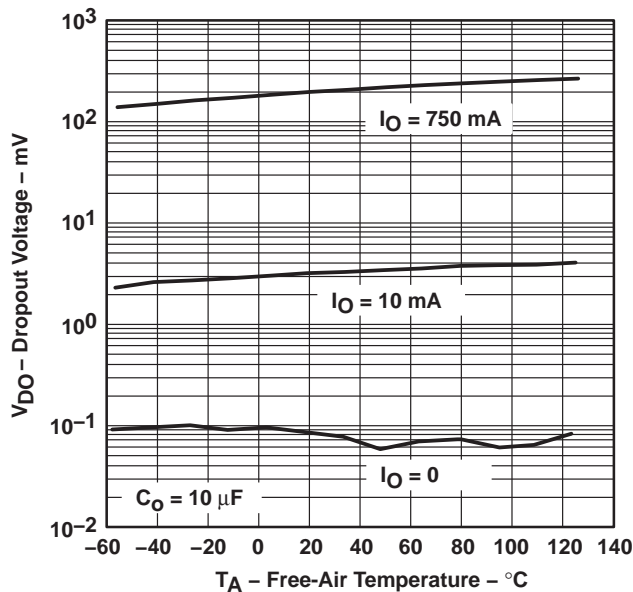


NC – No internal connection

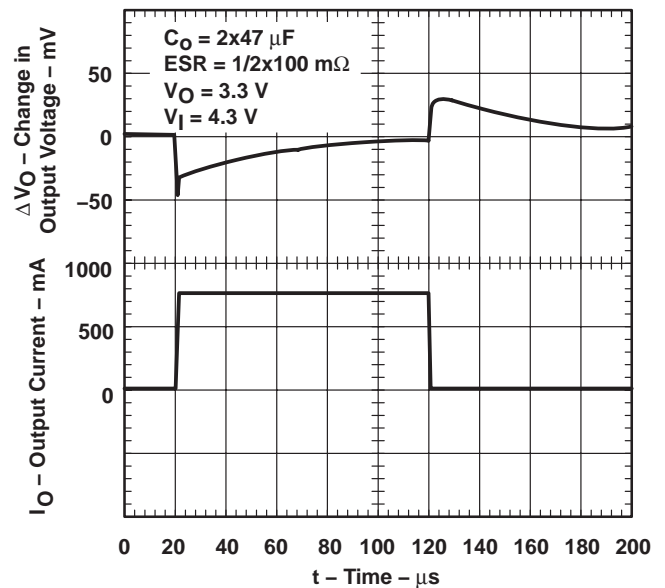
D PACKAGE
(TOP VIEW)



TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS77x33
LOAD TRANSIENT RESPONSE



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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 260 mV at an output current of 750 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 750 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μA at $T_J = 25^\circ\text{C}$.

The $\overline{\text{RESET}}$ output of the TPS777xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS777xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

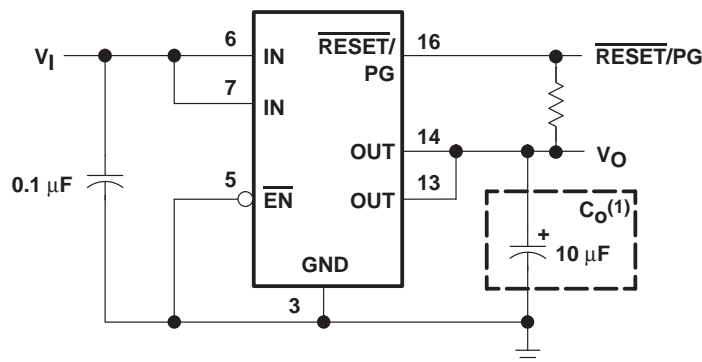
Power good (PG) of the TPS778xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS777xx and TPS778xx are offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for the TPS77701 option and 1.2 V to 5.5 V for the TPS77801 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS777xx and TPS778xx families are available in 8-pin SOIC and 20-pin PWP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES			
	TYP	TSSOP (PWP)		SOIC (D)	
-40°C to 125°C	3.3	TPS77733PWP	TPS77833PWP	TPS77733D	TPS77833D
	2.5	TPS77725PWP	TPS77825PWP	TPS77725D	TPS77825D
	1.8	TPS77718PWP	TPS77818PWP	TPS77718D	TPS77818D
	1.5	TPS77715PWP	TPS77815PWP	TPS77715D	TPS77815D
	Adjustable 1.5 V to 5.5 V	TPS77701PWP	—	TPS77701D	—
	Adjustable 1.2 V to 5.5 V	—	TPS77801PWP	—	TPS77801D

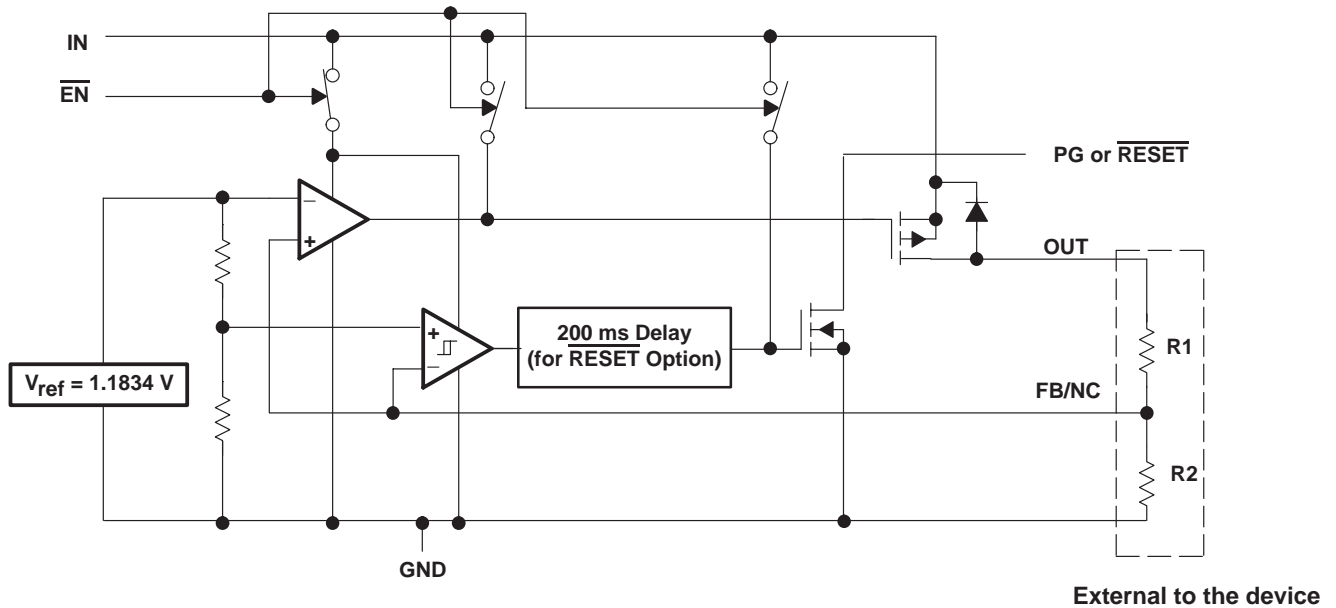
The TPS77x01 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS77701DR).



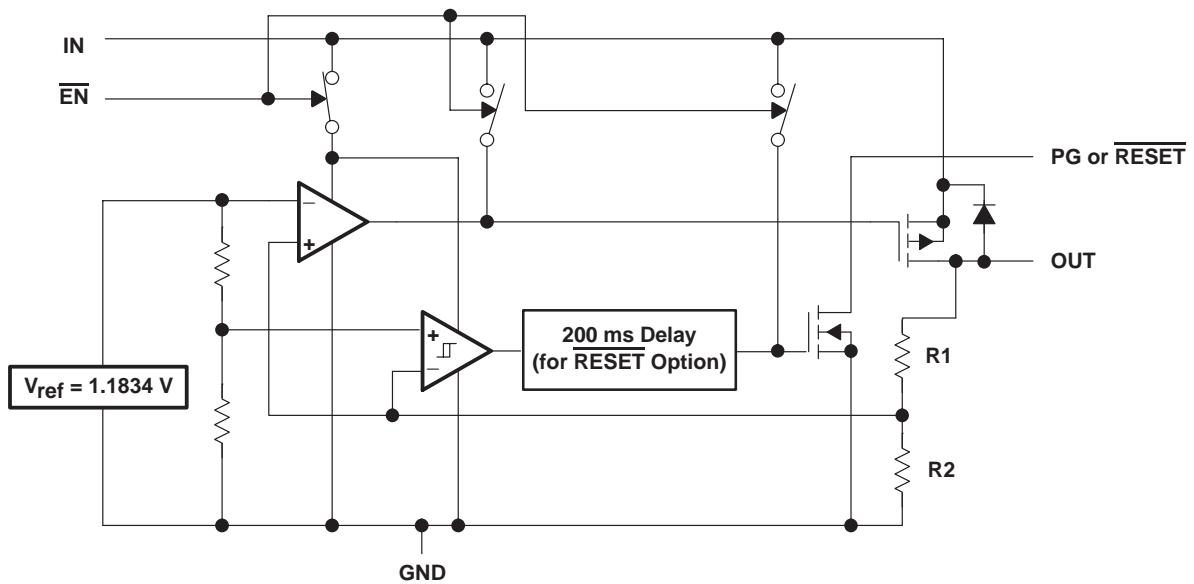
(1) See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 with $\overline{\text{RESET}}$ OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 with PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT LINEAR REGULATORS



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Terminal Functions

SOIC Package (TPS777xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{\text{RESET}}$	8	O	$\overline{\text{RESET}}$ output

TSSOP Package (TPS777xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{\text{RESET}}$	16	O	$\overline{\text{RESET}}$ output

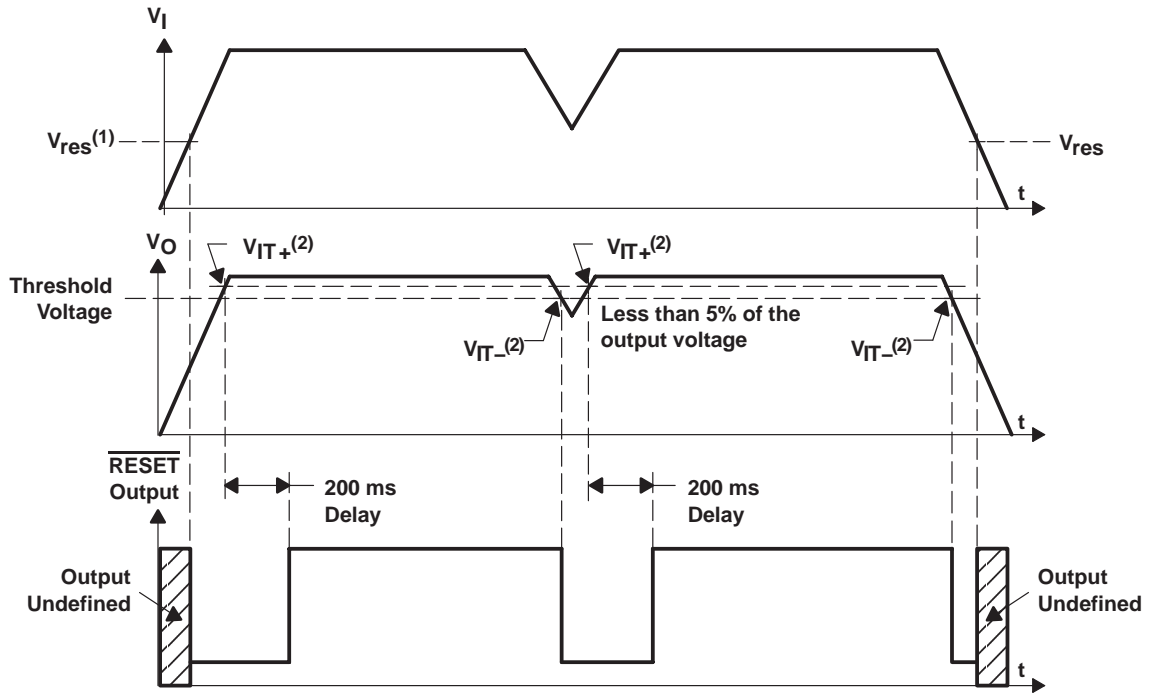
SOIC Package (TPS778xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
PG	8	O	PG output

TSSOP Package (TPS778xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output

TPS777xx $\overline{\text{RESET}}$ timing diagram



(1) V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT-} – Trip voltage is typically 5% lower than the output voltage ($95\%V_o$). V_{IT-} to V_{IT+} is the hysteresis voltage.

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 with RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 with PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT LINEAR REGULATORS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)(1)

Input voltage range ⁽²⁾ , V_I	-0.3 V to 13.5 V
Voltage range at EN	-0.3 V to 16.5 V
Maximum RESET voltage (TPS777xx)	16.5 V
Maximum PG voltage (TPS778xx)	16.5 V
Peak output current	Internally limited
Output voltage, V_O (OUT, FB)	7 V
Continuous total power dissipation	See dissipation rating tables
Operating junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
ESD rating, HBM	2 kV

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP§	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP¶	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

- (1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5 in × 5 in PCB, 1 oz. copper, 2 in × 2 in coverage (4 in²).
- (2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5 in × 2 in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I ⁽¹⁾		2.7	10	V
Output voltage range, V_O	TPS77701	1.5	5.5	V
	TPS77801	1.2	5.5	
Operating junction temperature, T_J		-40	125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.

electrical characteristics over recommended operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_I = V_{O(\text{typ})} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 750 mA load)	TPS77701	$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$, $T_J = 25^\circ\text{C}$	V_O			V
		$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$,	0.98 V_O	1.02 V_O		
	TPS77801	$1.2\text{ V} \leq V_O \leq 5.5\text{ V}$, $T_J = 25^\circ\text{C}$	V_O			
		$1.2\text{ V} \leq V_O \leq 5.5\text{ V}$,	0.98 V_O	1.02 V_O		
	TPS77x15	$T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_{IN} < 10\text{ V}$	1.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7\text{ V} < V_{IN} < 10\text{ V}$	1.470	1.530		
	TPS77x18	$T_J = 25^\circ\text{C}$, $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.8			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.764	1.836		
	TPS77x25	$T_J = 25^\circ\text{C}$, $3.5\text{ V} < V_{IN} < 10\text{ V}$	2.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5\text{ V} < V_{IN} < 10\text{ V}$	2.450	2.550		
	TPS77x33	$T_J = 25^\circ\text{C}$, $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.3			
		$T_J = -40^\circ\text{C}$ to 125°C , $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.234	3.366		
Quiescent current (GND current)		$10\text{ }\mu\text{A} < I_O < 750\text{ mA}$, $T_J = 25^\circ\text{C}$	85			μA
		$I_O = 750\text{ mA}$	125			
Output voltage line regulation ($\Delta V_O/V_O$)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$	0.01			%/V
Load regulation			3			mV
Output noise voltage (TPS77x18)		BW = 200 Hz to 100 kHz, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $I_C = 750\text{ }\mu\text{A}$	54			μVrms
Output current limit		$V_O = 0\text{ V}$	1.2	1.7	2	A
Thermal shutdown junction temperature			150			$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$, $T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_I < 10\text{ V}$	1			μA
		$\overline{\text{EN}} = V_I$, $2.7\text{ V} < V_I < 10\text{ V}$	10			μA
FB input current	TPS77x01	FB = 1.5 V	2			nA
High level enable input voltage			1.7			V
Low level enable input voltage			0.9			V
Power supply ripple rejection		$f = 1\text{ KHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$	60			dB
Reset (TPS77xx)	Minimum input voltage for valid $\overline{\text{RESET}}$	$I_O(\text{RESET}) = 300\text{ }\mu\text{A}$	1.1			V
	Trip threshold voltage	V_O decreasing	92	98		% V_O
	Hysteresis voltage	Measured at V_O	0.5			% V_O
	Output low voltage	$V_I = 2.7\text{ V}$, $I_O(\text{RESET}) = 1\text{ mA}$	0.15	0.4		V
	Leakage current	$V(\text{RESET}) = 5\text{ V}$	1			μA
	RESET time-out delay		200			ms

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 with $\overline{\text{RESET}}$ OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 with PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT LINEAR REGULATORS



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electrical characteristics over recommended operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_I = V_{O(\text{typ})} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG (TPS778xx)	Minimum input voltage for valid PG	$I_{O(\text{PG})} = 300\text{ }\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	$\%V_O$
	Hysteresis voltage	Measured at V_O		0.5		$\%V_O$
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{O(\text{PG})} = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{PG}) = 5\text{ V}$			1	μA
Input current ($\overline{\text{EN}}$)		$\overline{\text{EN}} = 0\text{ V}$	-1	0	1	μA
		$\overline{\text{EN}} = V_I$	-1		1	
Dropout voltage (1)	TPS77733	$I_O = 750\text{ mA}$, $T_J = 25^\circ\text{C}$		260		mV
		$I_O = 750\text{ mA}$,			427	
	TPS77833	$I_O = 750\text{ mA}$, $T_J = 25^\circ\text{C}$		260		
		$I_O = 750\text{ mA}$,			427	

(1) IN voltage equals $V_{O(\text{typ})} - 100\text{ mV}$; TPS77x01 output voltage set to 3.3 V nominal with external resistor divider. TPS77x15, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
Z_O	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Input voltage (min)	vs Output voltage	14
	Line transient response		15, 17
	Load transient response		16, 18
V_O	Output voltage	vs Time	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24

TYPICAL CHARACTERISTICS

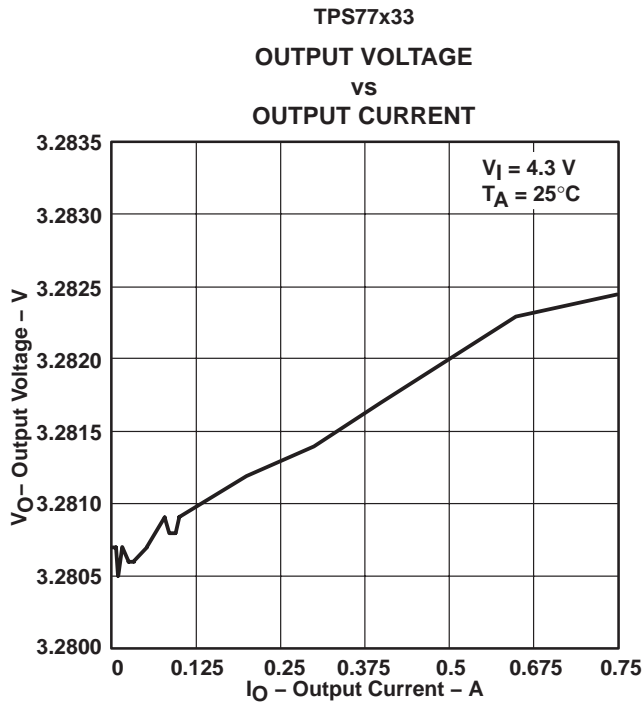


Figure 2

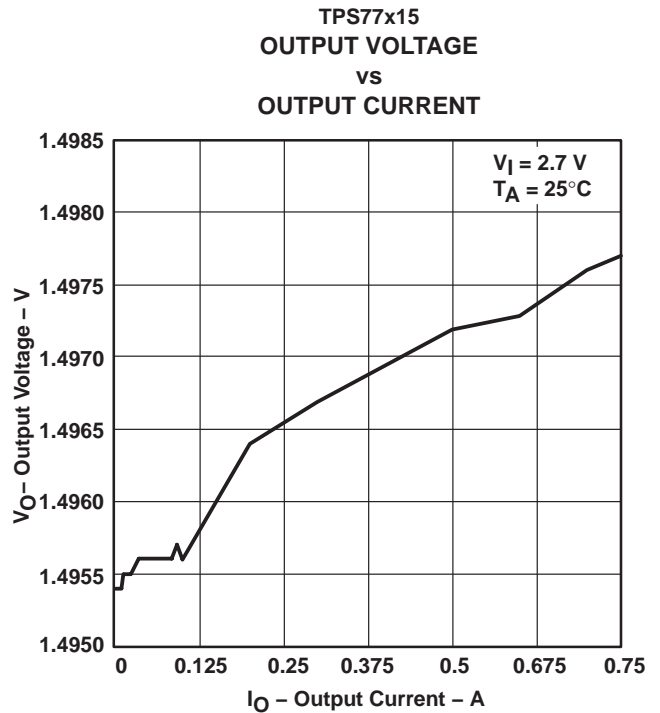


Figure 3

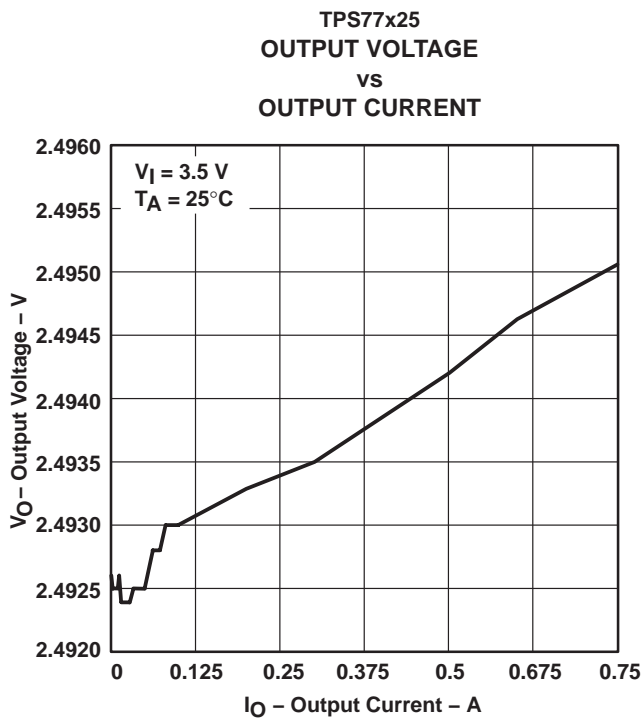


Figure 4

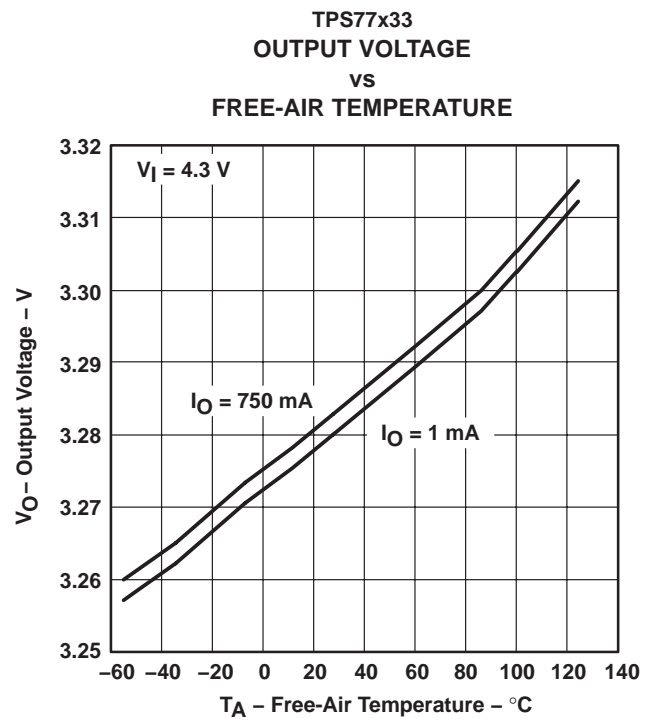


Figure 5

TYPICAL CHARACTERISTICS

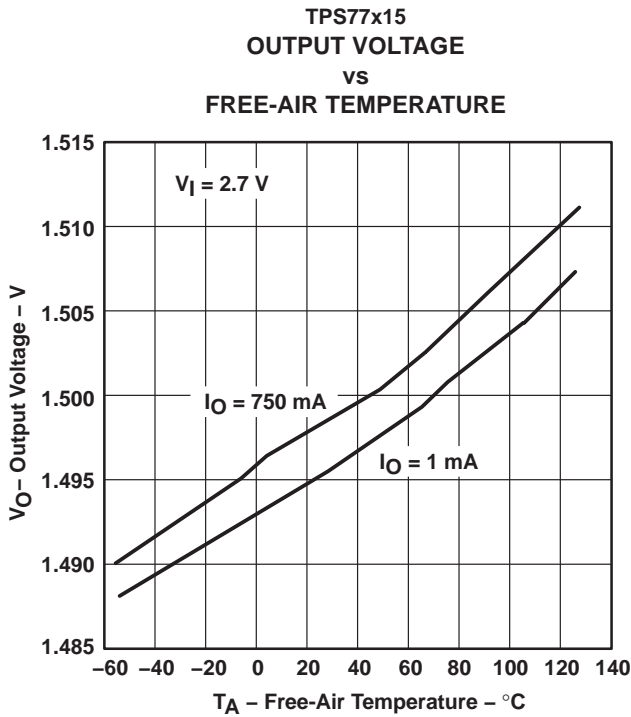


Figure 6

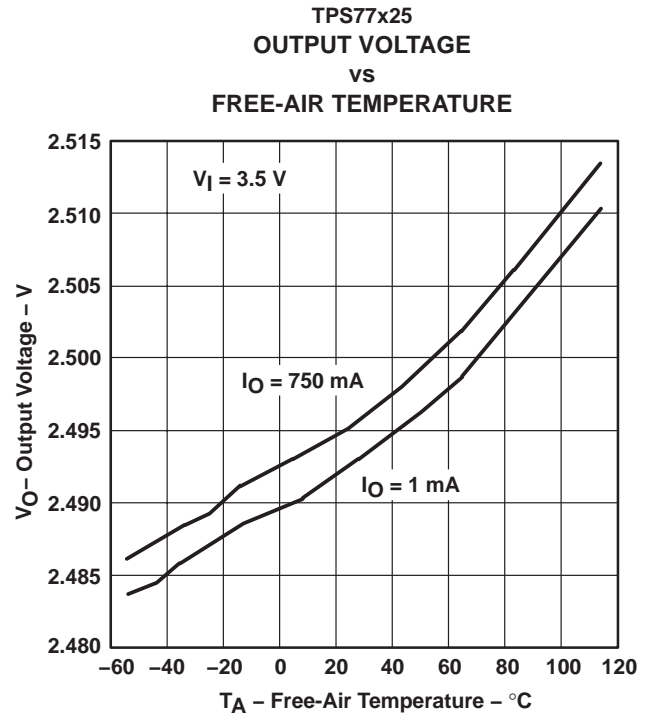


Figure 7

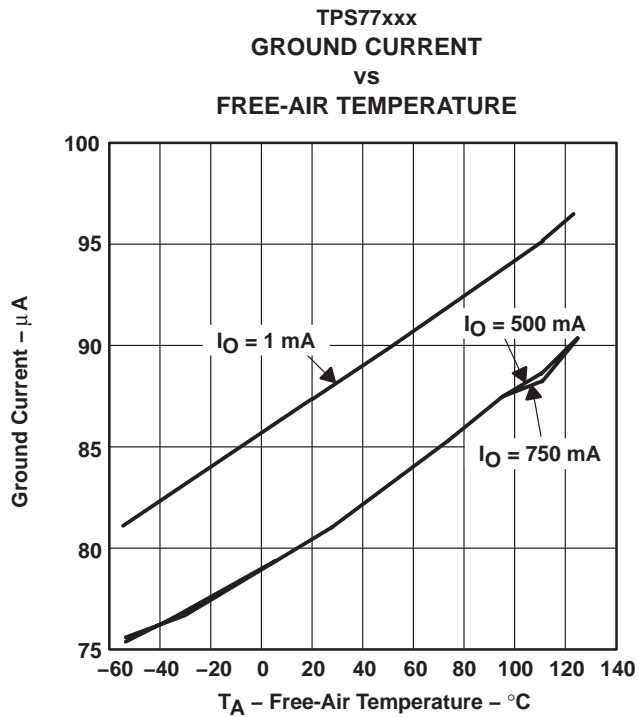


Figure 8

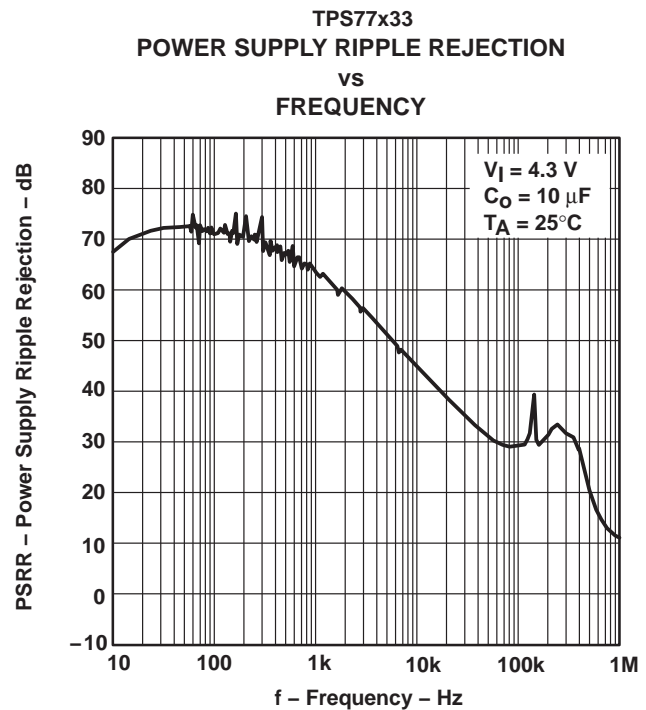


Figure 9

TYPICAL CHARACTERISTICS

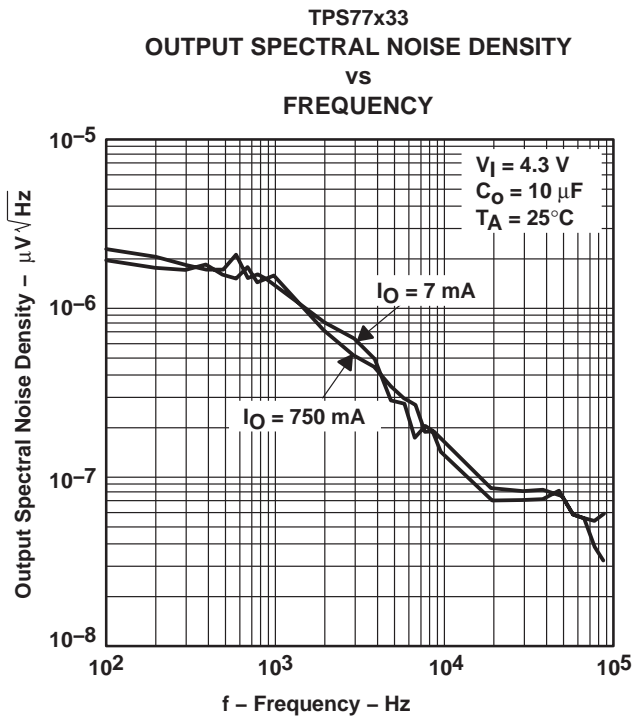


Figure 10

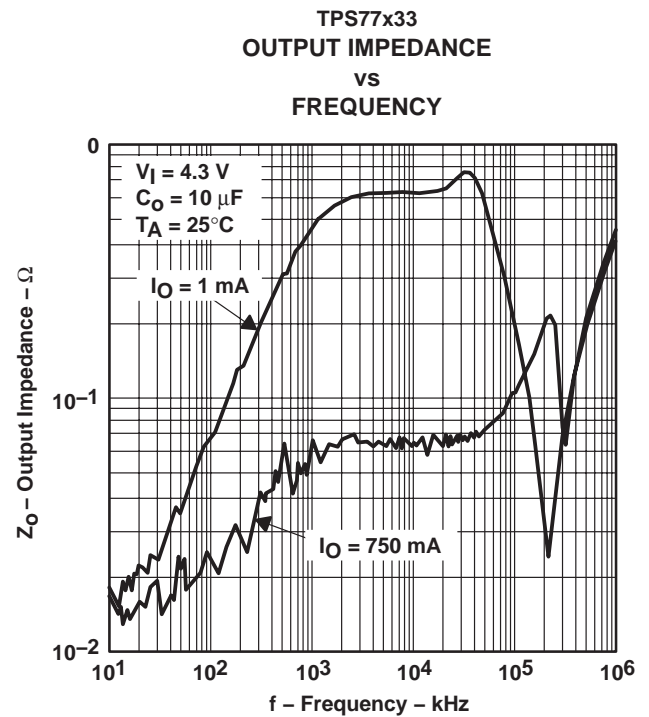


Figure 11

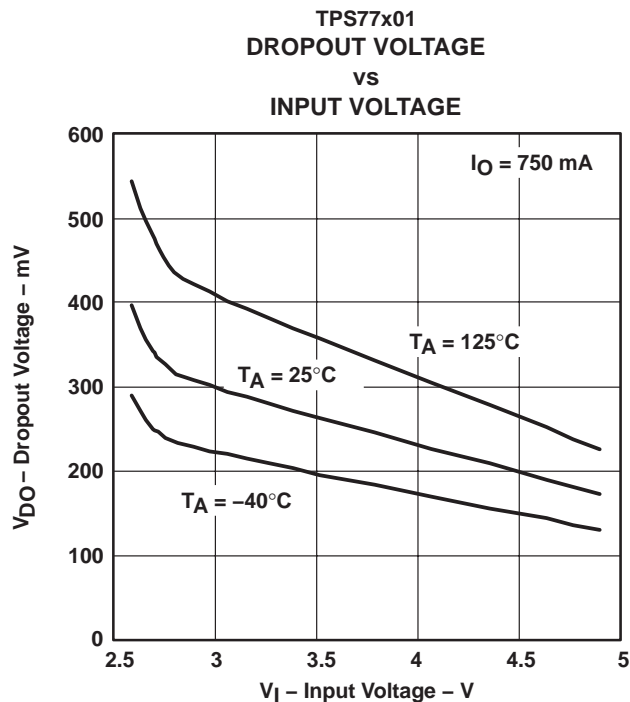


Figure 12

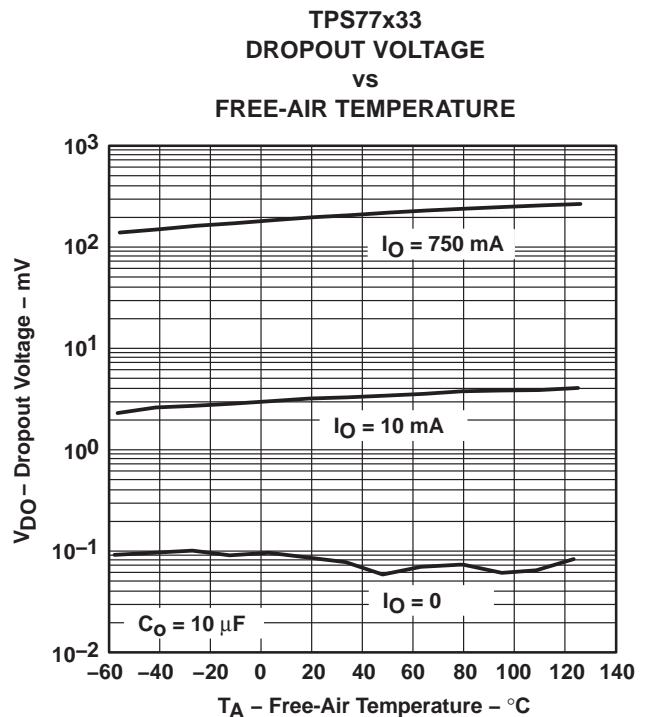


Figure 13

TYPICAL CHARACTERISTICS

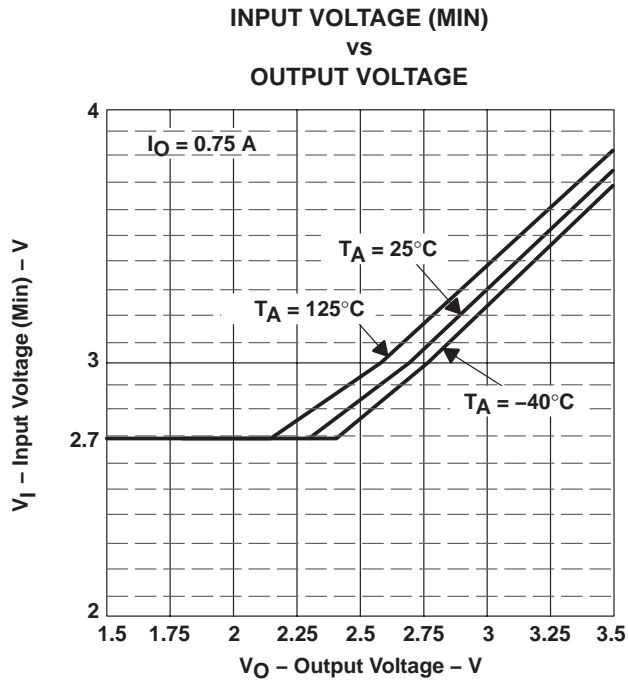


Figure 14

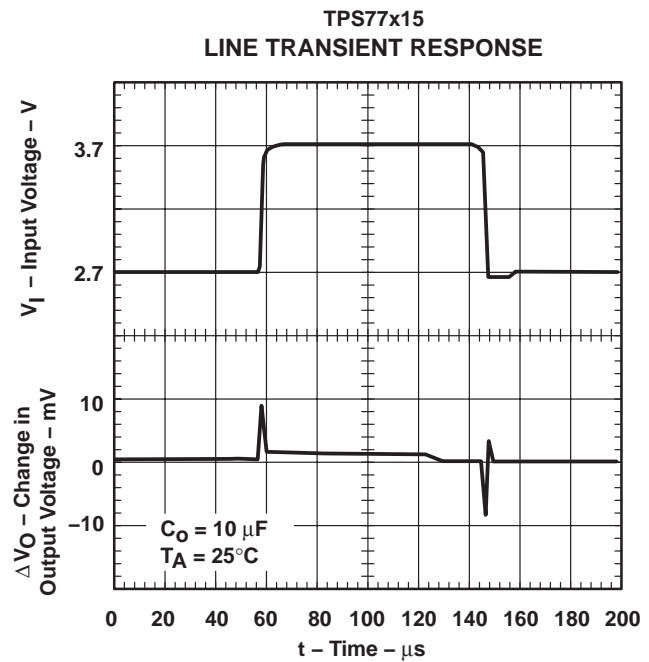


Figure 15

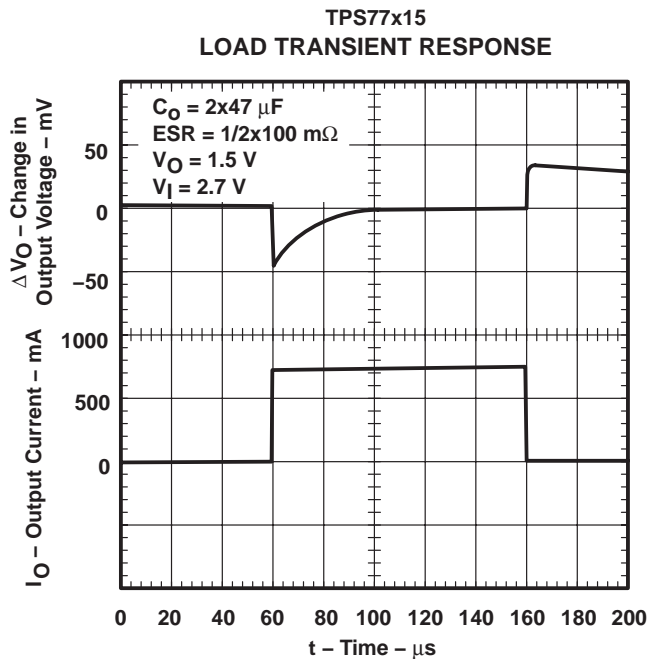


Figure 16

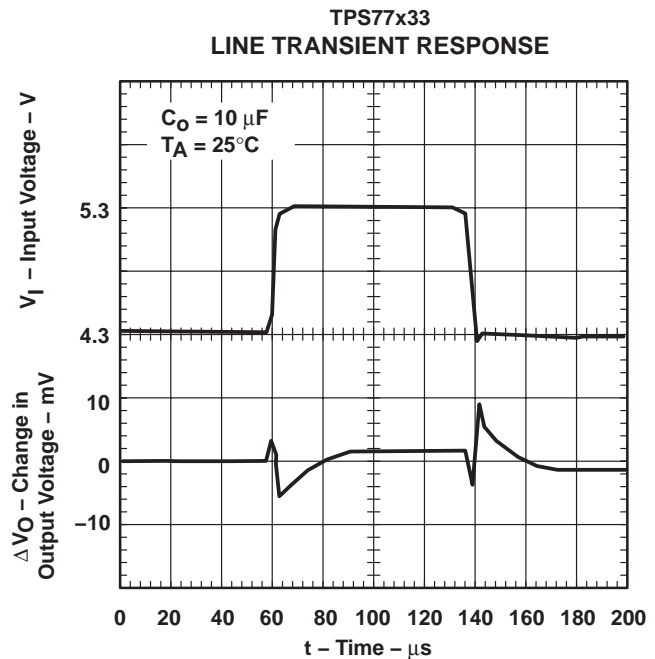


Figure 17

TYPICAL CHARACTERISTICS

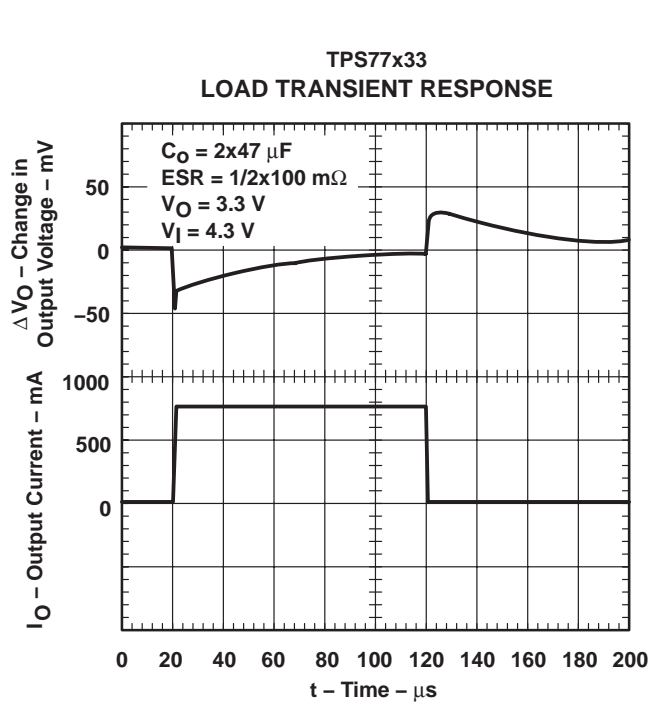


Figure 18

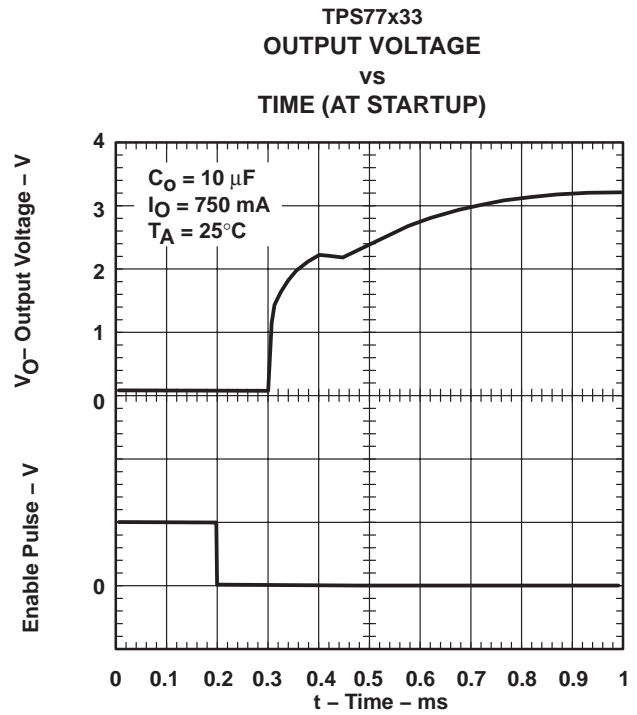


Figure 19

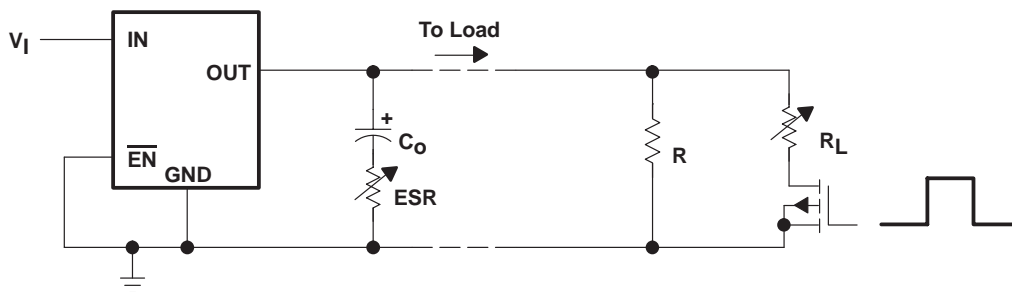


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

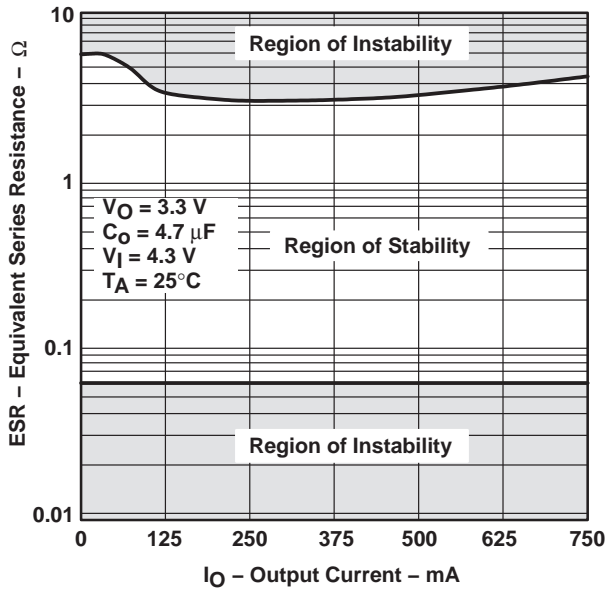


Figure 21

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

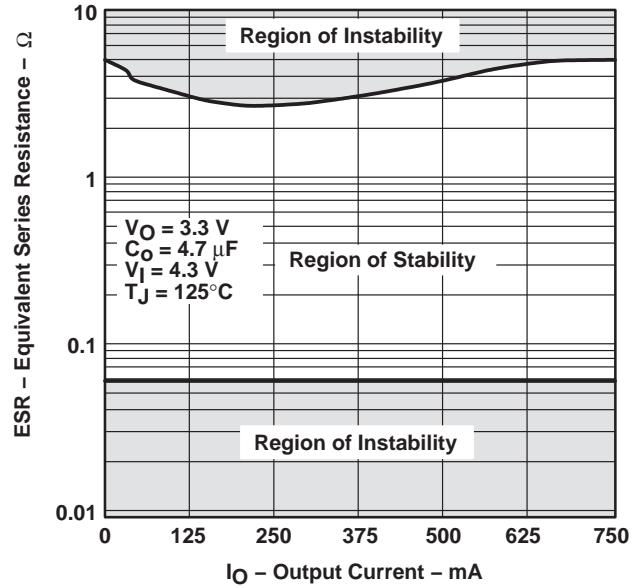


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

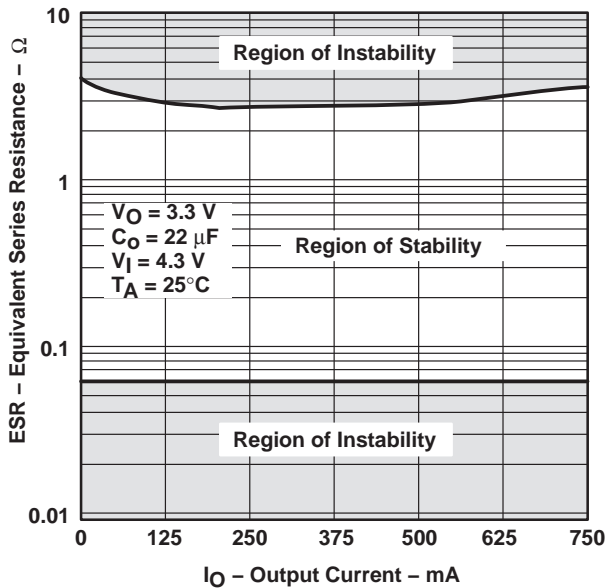


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE(1)
 vs
 OUTPUT CURRENT

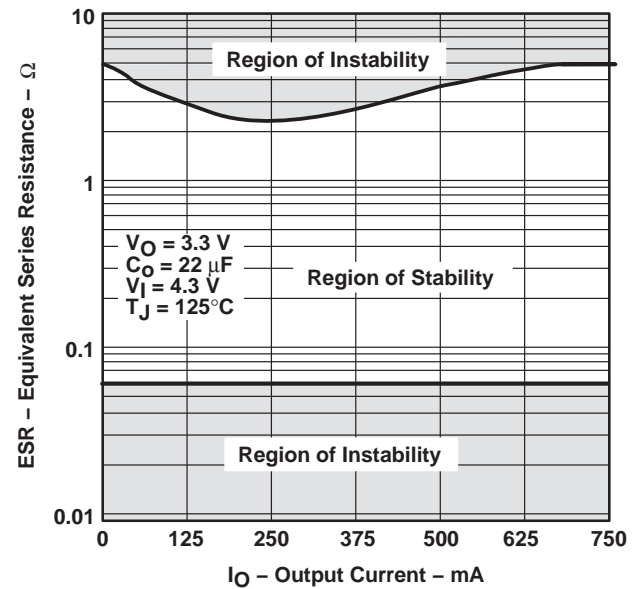


Figure 24

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

APPLICATION INFORMATION

The TPS777xx and TPS778xx families include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77x01 (adjustable from 1.5 V to 5.5 V for TPS77701 option and 1.2 V to 5.5 V for TPS77801 option).

device operation

The TPS777xx and TPS778xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS777xx and TPS778xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS777xx and TPS778xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS777xx and TPS778xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μA . If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground.

minimum load requirements

The TPS777xx and TPS778xx families are stable even at zero load; no minimum load is required for operation.

FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS777xx or TPS778xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS777xx and TPS778xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

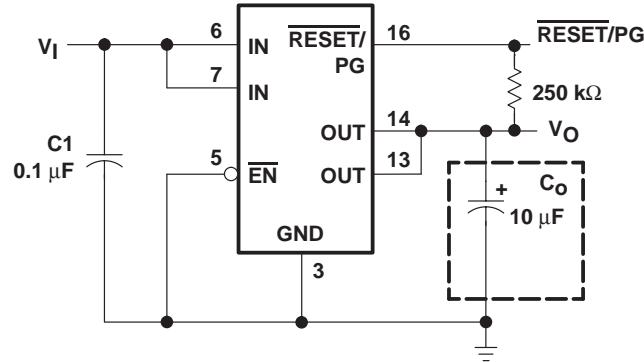


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

$V_{ref} = 1.1834 \text{ V typ}$ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose $R2 = 110 \text{ k}\Omega$ to set the divider current at approximately 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

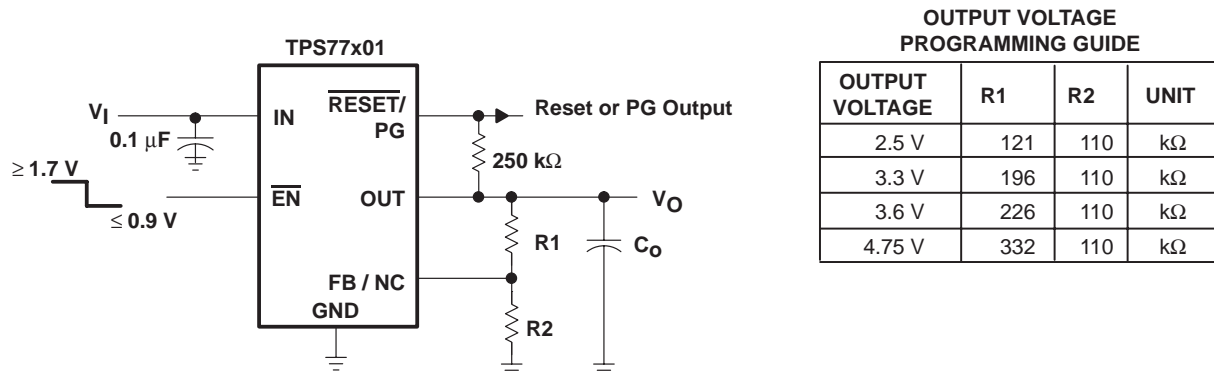


Figure 26. TPS77x01 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

reset indicator

The TPS777xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

power-good indicator

The TPS778xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS777xx and TPS778xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS777xx and TPS778xx also feature internal current limiting and thermal protection. During normal operation, the TPS777xx and TPS778xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

APPLICATION INFORMATION

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\max)} = \frac{T_{J\max} - T_A}{R_{\theta JA}}$$

Where:

$T_{J\max}$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, and is calculated as

$$\frac{1}{\text{derating factor}} \quad \text{from the dissipation rating tables.}$$

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS77701D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77701DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77701DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77701DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77701PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77701PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77701PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77701PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77715D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77715DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77715DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77715DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77715PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77715PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77718D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77718DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77718DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77718DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77718PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77718PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77718PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77718PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77725D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77725DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77725DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS77725DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77725PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77725PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77725PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77725PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77733D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77733DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77733DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77733DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77733PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77733PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77733PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77733PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77801D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77801DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77801DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77801DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77801PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77801PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77801PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77801PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77815D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77815DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77815DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77815DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77815PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS77815PWP4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77815PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77815PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77818D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77818DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77818PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77818PWP4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77818PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77818PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77825D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77825DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77825DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77825DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77825PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77825PWP4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77825PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77825PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77833D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77833DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77833DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77833DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77833PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77833PWP4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77833PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS77833PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



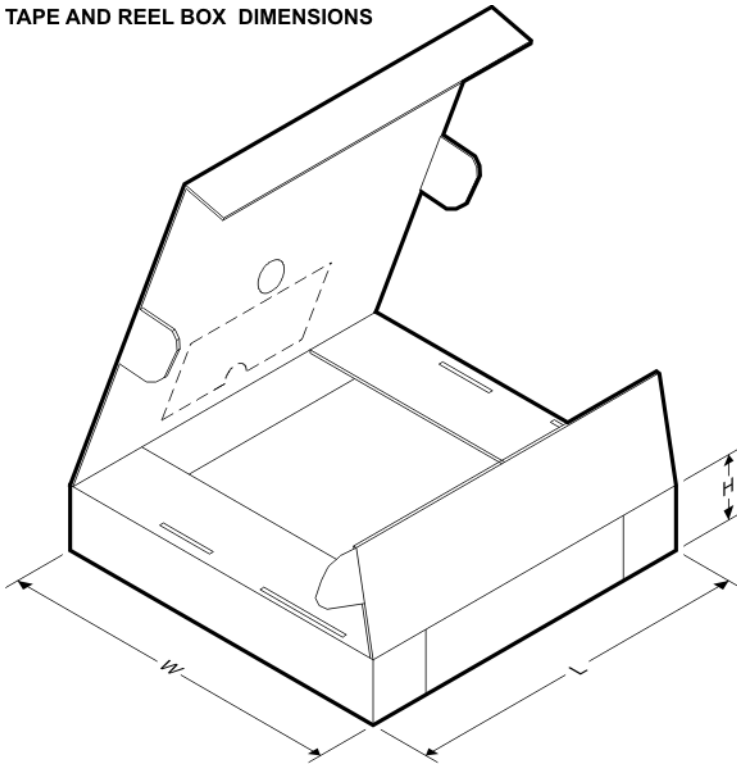
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77701DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77701PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77715DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77718DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77718PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77725DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77725PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77733DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77733PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77801DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77801PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77815DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77815PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77818PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77825DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77825PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77833PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

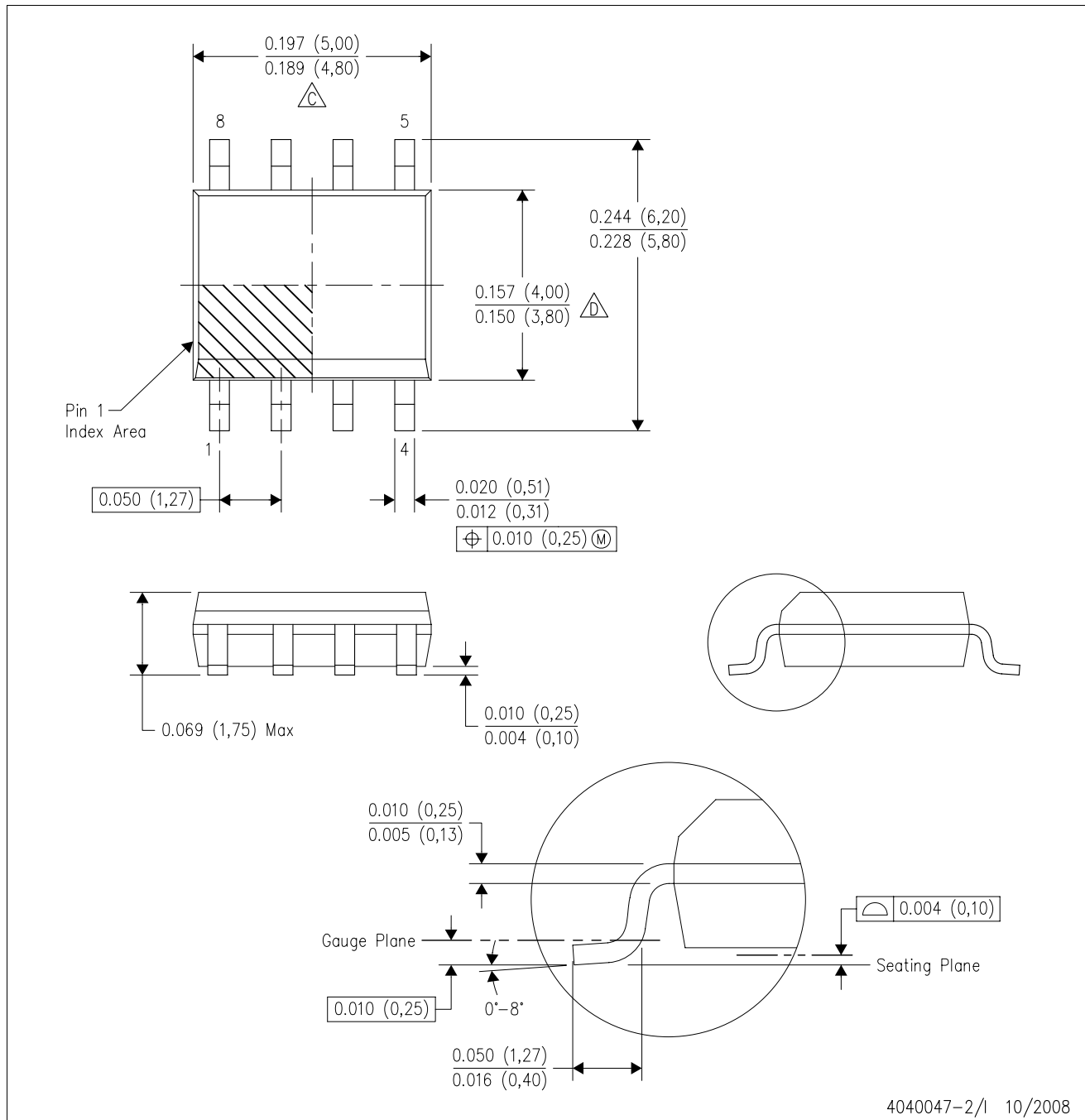


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77701DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77701PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77715DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77718DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77718PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77725DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77725PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77733DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77733PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77801DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77801PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77815DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77815PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77818PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77825DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77825PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS77833DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS77833PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0

D (R-PDSO-G8)

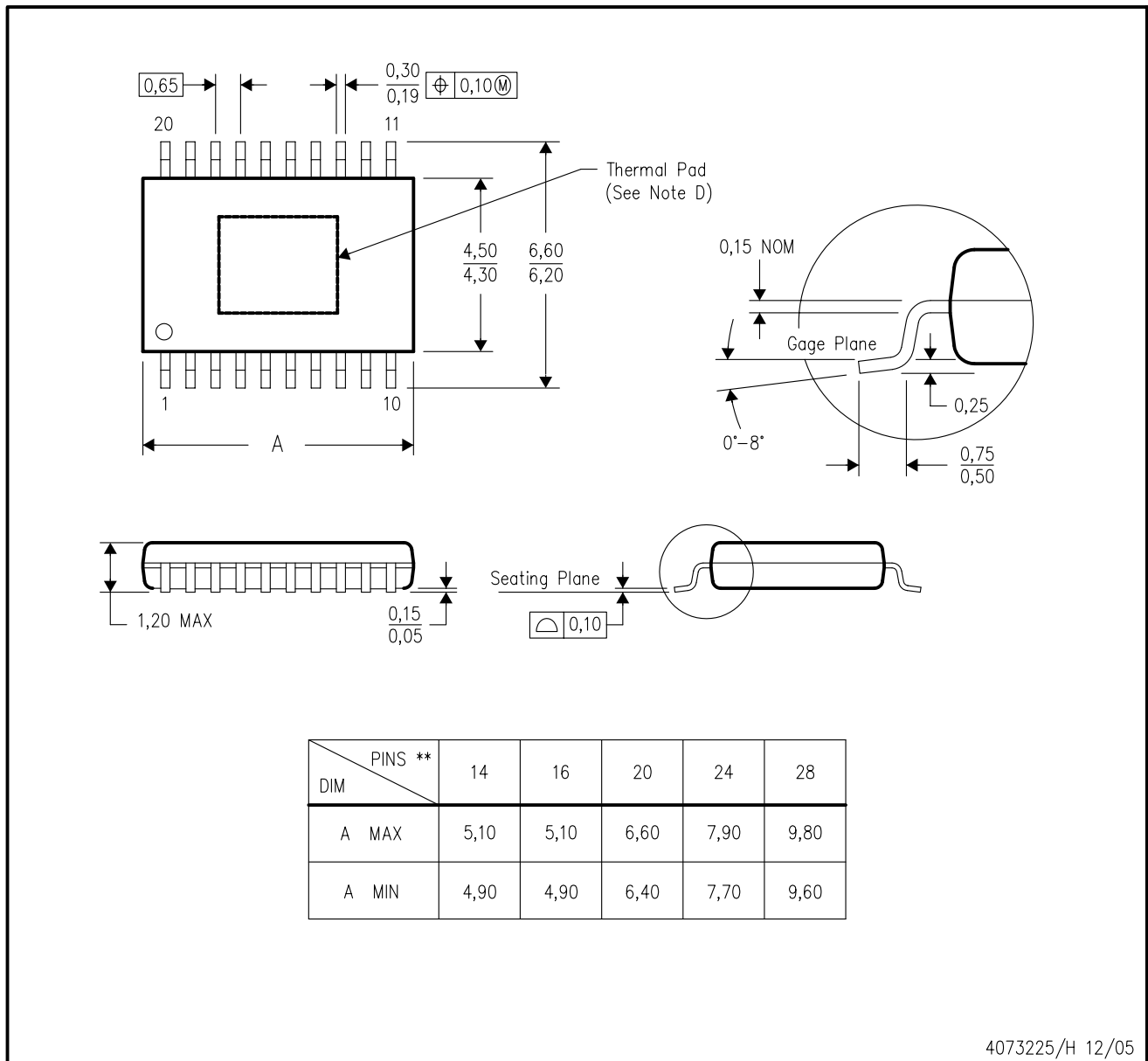
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

PWP (R-PDSO-G**) 20 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073225/H 12/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-153

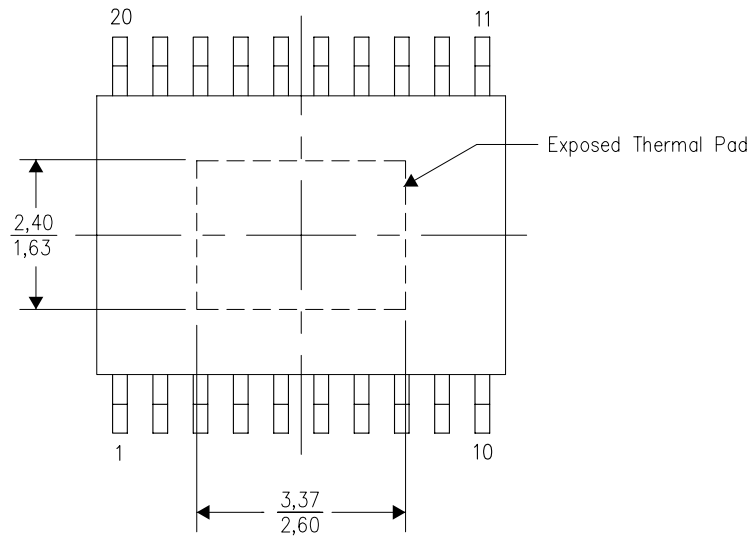
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

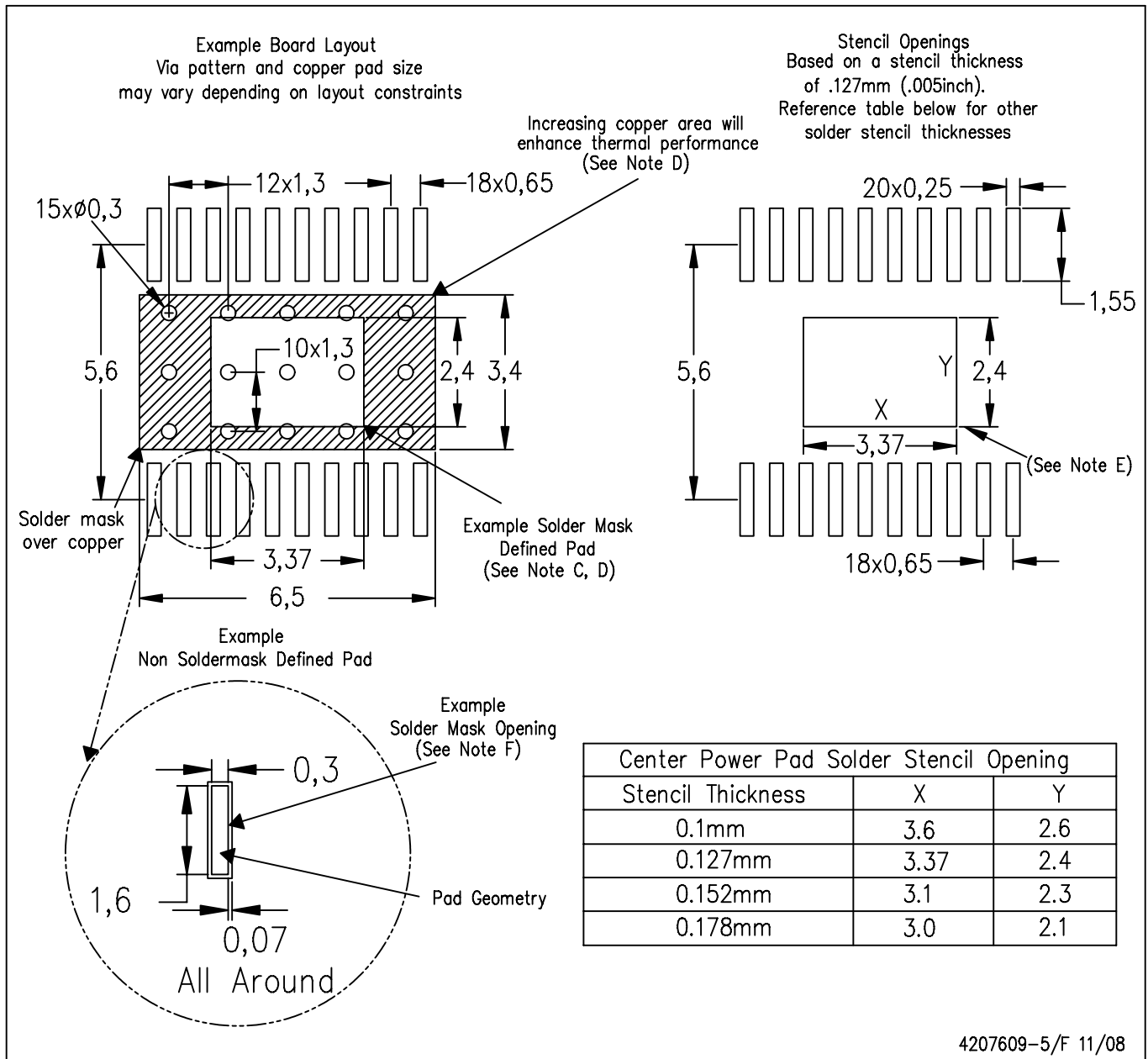


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G20) PowerPAD™



4207609-5/F 11/08

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

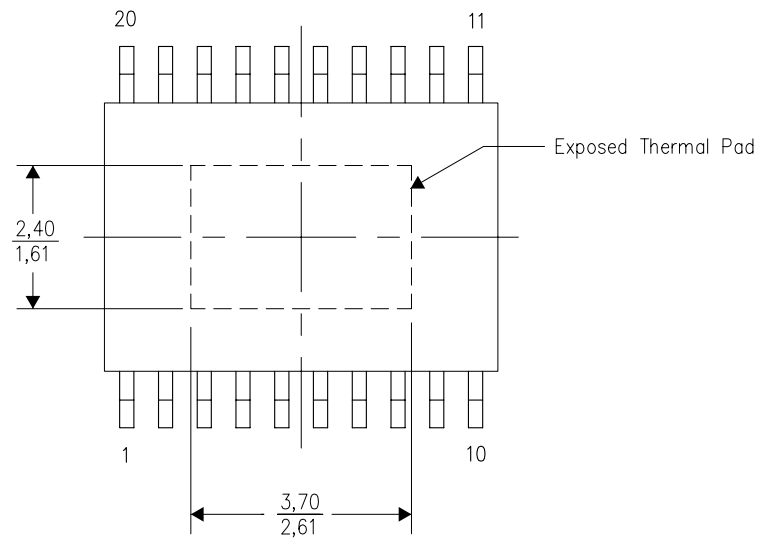
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THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.

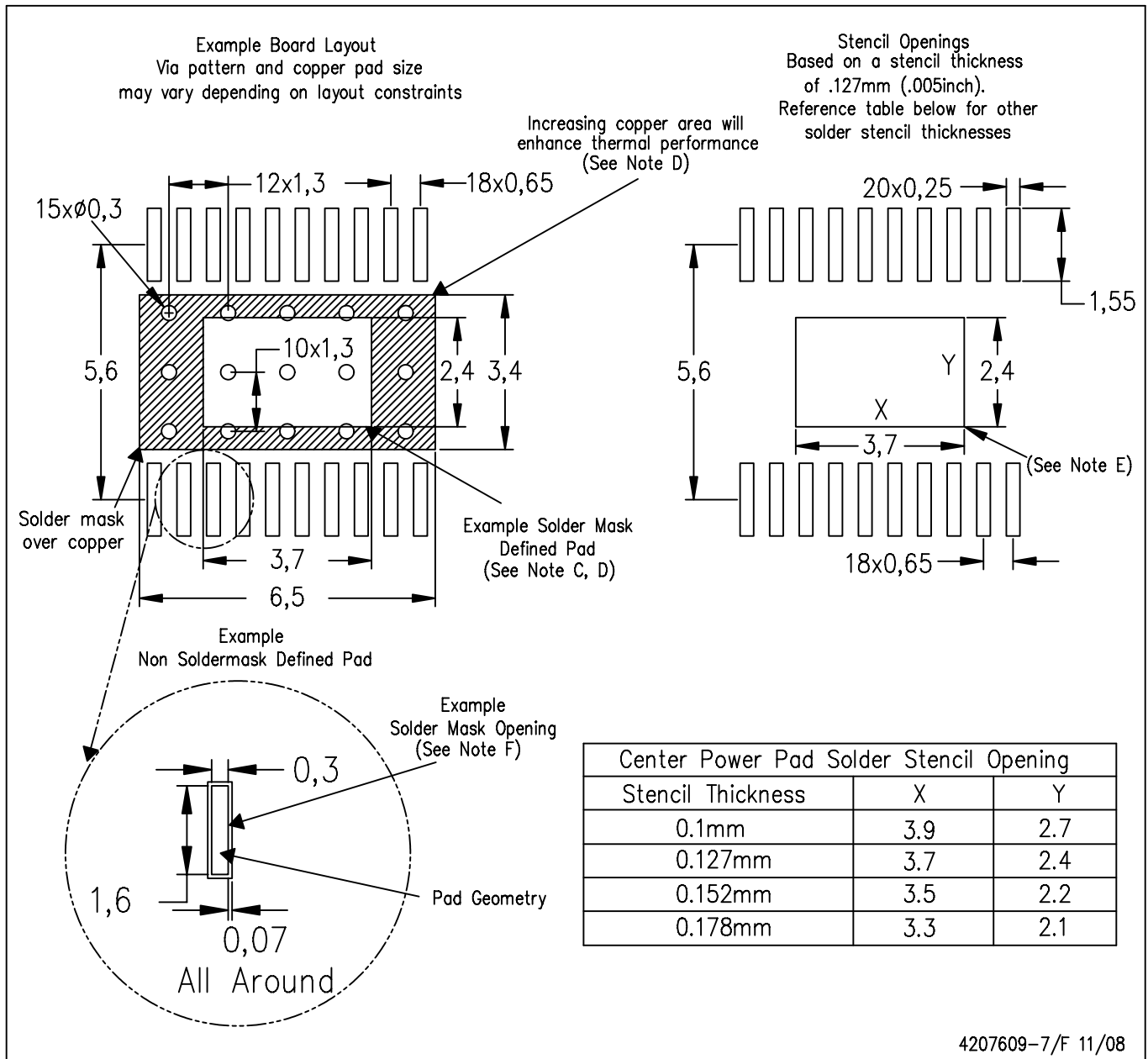


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G20) PowerPAD™



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
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